

EE4306 RF Design Assignment

Diplexer

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1 Introduction

The task was to design a diplexer to separate UHF and VHF RF frequencies at a crossover frequency of 470 MHz. The circuit should have three terminals: an output covering the whole frequency range and two inputs being a low frequency (VHF) input and a high frequency (UHF) input. The output impedance is to be matched to $50\ \Omega$ with an s_{11} of less than -15 dB for frequencies between 141 MHz (0.3 times the crossover frequency) and 1410 MHz (3 times the crossover frequency). The signal at the output due to the high pass input should be greater than -3 dB of the input signal for all frequencies above the specified crossover frequency and three times that frequency (1410 MHz). The signal at the output due to the low pass input should be greater than -3 dB of the input signal for all frequencies from 141 MHz and up to 470 MHz (crossover frequency).

To minimise the cost, the diplexer is to be made on FR3 PCB with capacitors used as the only components. The capacitors had to be made up with standard value capacitors. All the inductors should be made using printed circuit board techniques and can include transmission lines. The material properties of the FR3 board can be found in table 1. The dielectric constant and thickness are not controlled well and can vary by 5%. The design should allow for this variation.

thickness of the dielectric material	1.5s mm
relative dielectric constant	3.2
loss tangent	0.02
Copper cladding	1 oz (0.035 mm)

Table 1: FR3 PCB board - material properties

PCB mounting BNC connectors had to be used as the connectors to get the signals in and out of the board.

2 Design

2.1 Basis design

The basic design for the diplexer consists of a highpass and a lowpass which will be combined. A 4th order Butterworth filter was used because it ensures a flat response in the pass band and an adequate rate roll off. Figure 1 shows the principle of such a circuit with the lowpass filter on the bottom and the highpass filter on top.

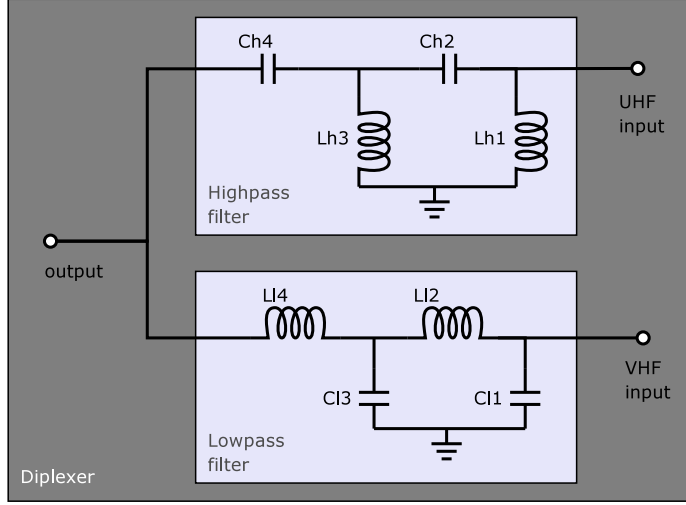


Figure 1: Diplexer with 4th order Butterworth filter

To calculate the appropriate values of the conductors and inductors for this filter, the equation 1 was used to derive the normalised values of L or C. After this, the equations 2 to 5 on the current page were used to calculate both inductivity and conductance.

$$LC_{inormalised} = 2 \sin\left((2i - 1) \frac{\pi}{8}\right) \quad i = 1, 2, \dots, 4 \quad (1)$$

and for the high and low pass filter

$$L_{ihighpass} = \frac{R}{2\pi F_c LC_{inormalised}} \quad i = 1, 2 \quad (2)$$

$$C_{ihighpass} = \frac{1}{2\pi F_c R LC_{inormalised}} \quad i = 2, 4 \quad (3)$$

$$L_{ilowpass} = \frac{LC_{inormalised} R}{2\pi F_c} \quad i = 2, 4 \quad (4)$$

$$C_{ilowpass} = \frac{LC_{inormalised}}{2\pi F_c R} \quad i = 1, 2 \quad (5)$$

R is the load impedance = 50 Ω

F_c is the desired cut off frequency = 470 MHz

Element	Normalised	Highpass	Lowpass
1	0.765367	$L_{h1} = 22.117 * 10^{-9} H$	$C_{l1} = 5.185 * 10^{-12} F$
2	1.847759	$C_{h2} = 3.665 * 10^{-12} F$	$L_{l2} = 31.285810^{-9} H$
3	1.847759	$L_{h3} = 9.163 * 10^{-9} H$	$C_{l3} = 12.514 * 10^{-12} F$
4	0.765367	$C_{h4} = 8.847 * 10^{-12} F$	$L_{l4} = 12.961 * 10^{-9} H$

Table 2: Start values for the diplexer

The derived values can be found in table 2 and were used to create a circuit for a first simulation. Because this circuit did not perform in the given limits, a first optimisation was done. The resulting modified circuit with its element values is shown in figure 2 on the next page. The frequency response of this circuit is displayed in figure 3 on the following page.

The result is a basic diplexer which is suitable for the given limits. This can be used for the next step where all inductors were substituted with transmission lines.

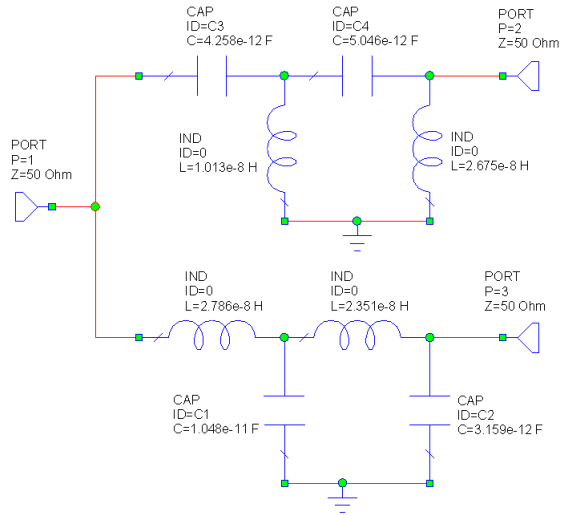


Figure 2: Diplexer schematic after optimisation

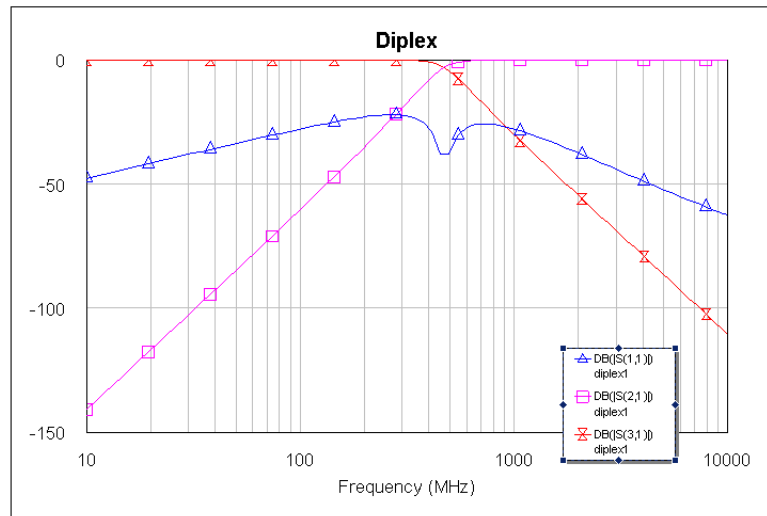


Figure 3: Frequency response of the diplexer

2.2 Printed circuit board design

The printed circuit board design has been started with the element values from section 2.1 on page 3 shown in figure 2 on the preceding page. First, a MSUB substrate with the given attributes was added to the schematic. After this, all inductors were changed to transmission lines.

Now the optimiser was used to calculate the length of the transmission lines. It ended up with just convenient lengths for the transmission lines and practical values for the capacitors, shown in the schematic on figure 4 on the next page. The frequency response of the current circuit can be found in figure 5 on the following page

Some additional transmission lines had to be added to implement the circuit. For example, to be able to solder an BNC connector to every port, it is necessary to add an 6x3 mm copper transmission line. Furthermore, adequate tapers and additional transmission lines were added between the condensators of the highpass filter to give more space for the transmission lines of the lowpass filter.

After this new optimisation, the lumped element condensators were substituted by standard sized condensators from ATC (series 100a) this condensators could not achieve exactly the same values as before, another optimisation step was needed. Having done this, the transmission lines of the highpass filter had again to be adapted - this time to the now known width of the condensators.

The values of the conductors can be found in table 3 (labelled as in figure 7 on page 8).

Conductor (ATC - 100a)	Size
C_{l1}	3.3 pF
C_{l3}	10 pF
C_{h2}	4.7 pF
C_{h4}	4.3 pF

Table 3: Values of the standard conductors

It was required to fit the circuit in the smallest possible space. Thus, additional bends had to be added to the transmission lines. Hence, the long lines of the lowpass filter were laid like a snake. Because there must not be any interference between two transmission lines, I used a small schematic to calculate the minimum distance, using a coupled line and comparing its frequency response with the one of a simple transmission line until there was no difference detectable, anymore. So, it could be determined that a distance of 3 mm is sufficiently save enough. This was taken into account during the final layout process which resulted in figure 6 on page 8.

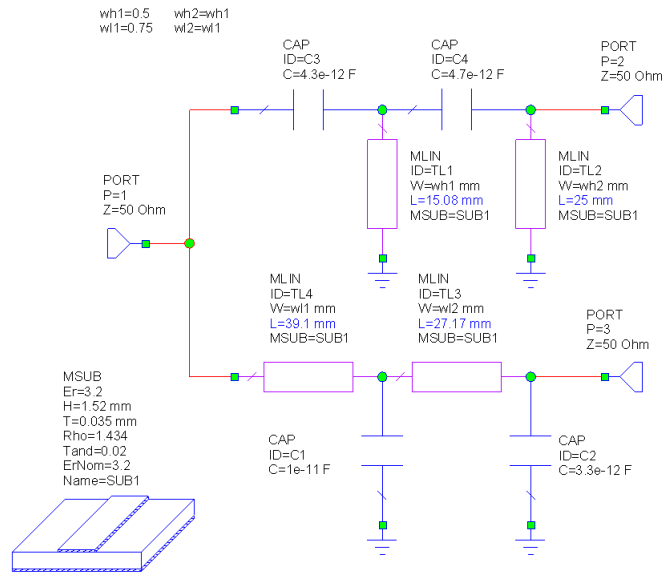


Figure 4: Schematic with transmission lines instead of inductors

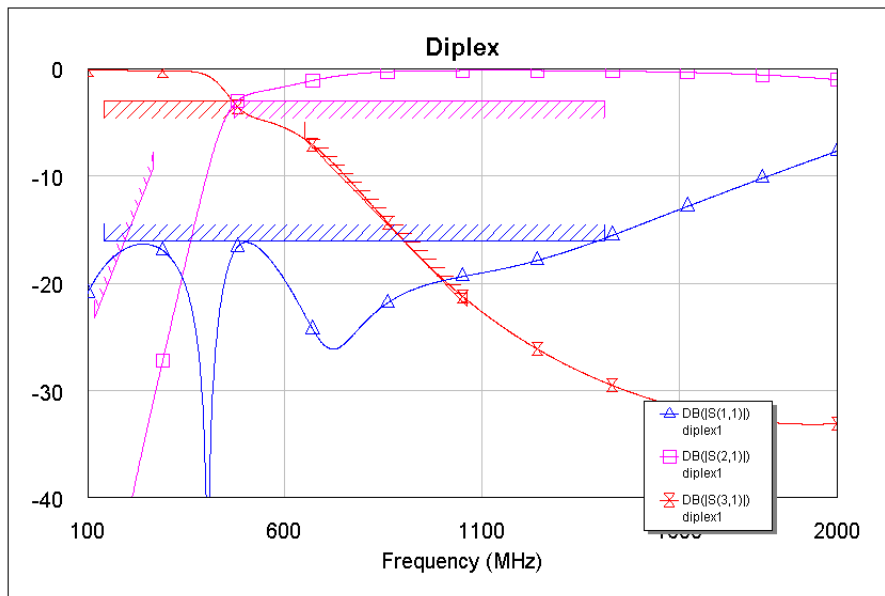


Figure 5: Frequency response with transmission lines instead of inductors

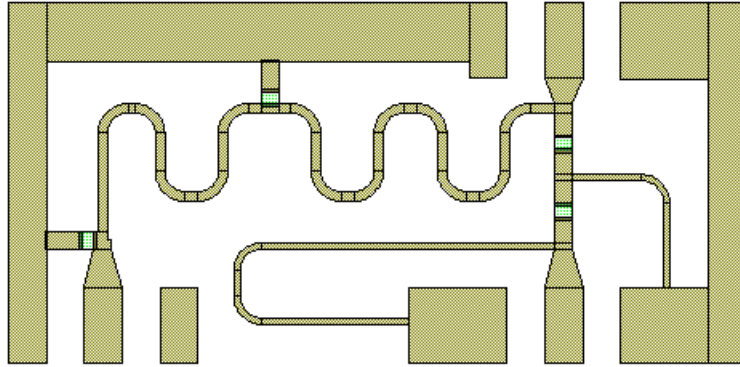


Figure 6: Final layout

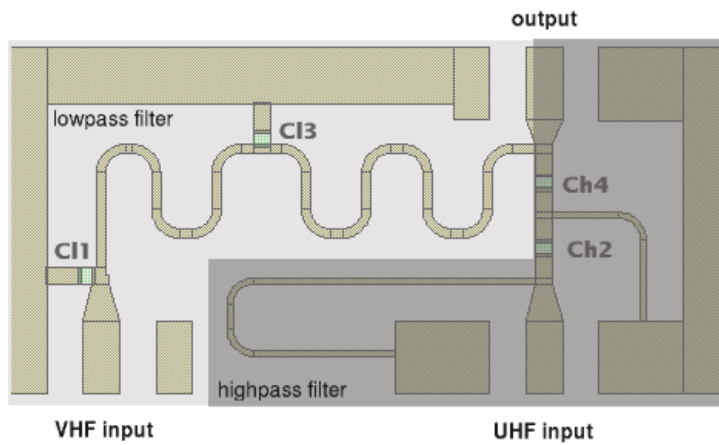


Figure 7: Final layout - schematically

3 Verification

To ensure the board will comply with the specifications, even if the dielectric constant and the thickness of the board vary, both values were turned to tunable. After changing these values to the given limits ($\pm 5\%$) it became obvious that the combination of the maximum thickness and the minimal dielectric constant is the worst case scenario for the circuit. Therefore, the circuit was optimised again for this attributes of the substrate. The result can be seen in figure 9 on page 10.

After the circuit did fit into all the specifications, it was checked again over the bandwidths of both parameters and behaved as expected.

Even with the frequency response of the circuit (figure 10 on page 10) not looking that good over the whole bandwidth, in the limits of the specifications it still works as it is supposed to do. Therefore this should be no problem at all.

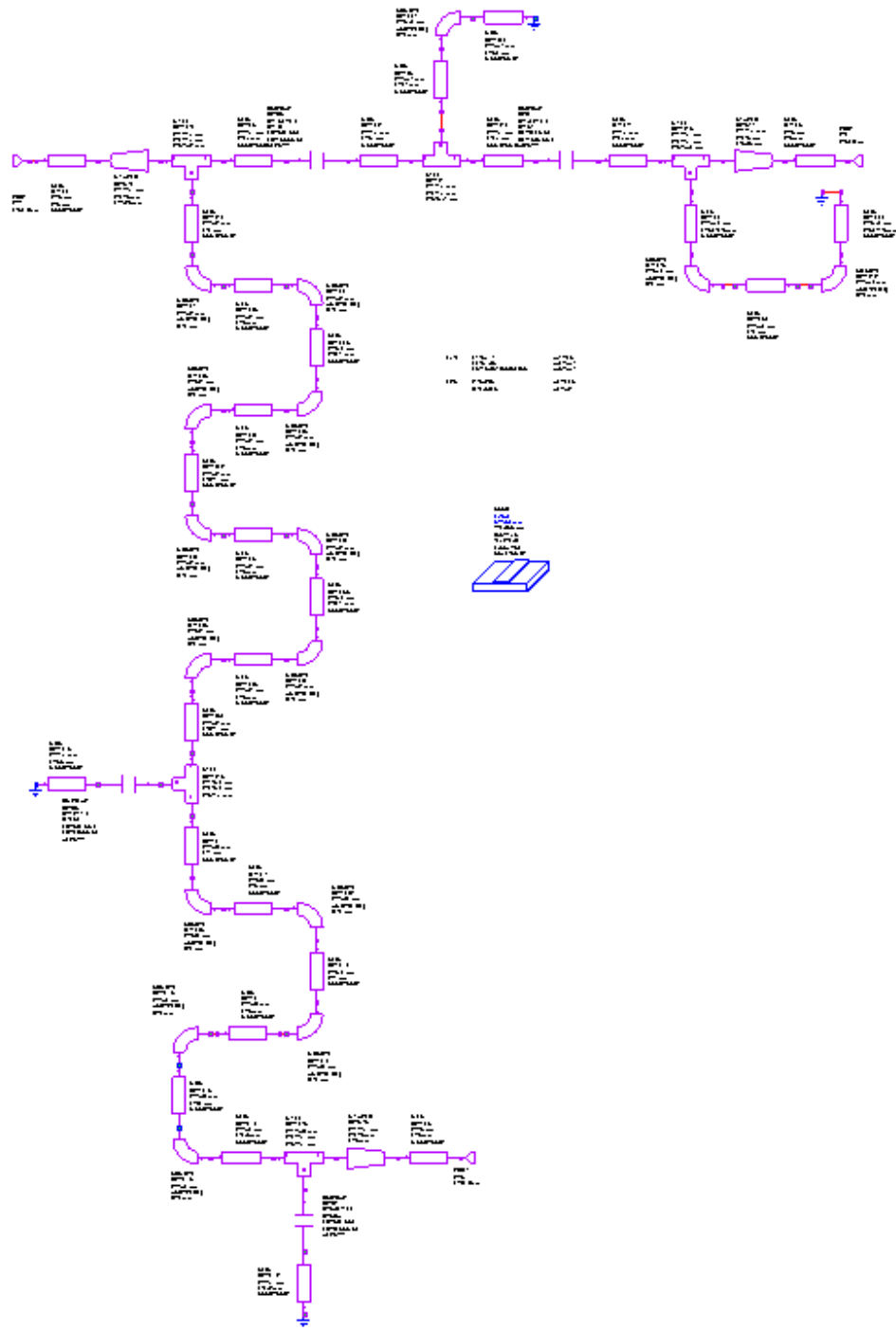


Figure 8: Schematic

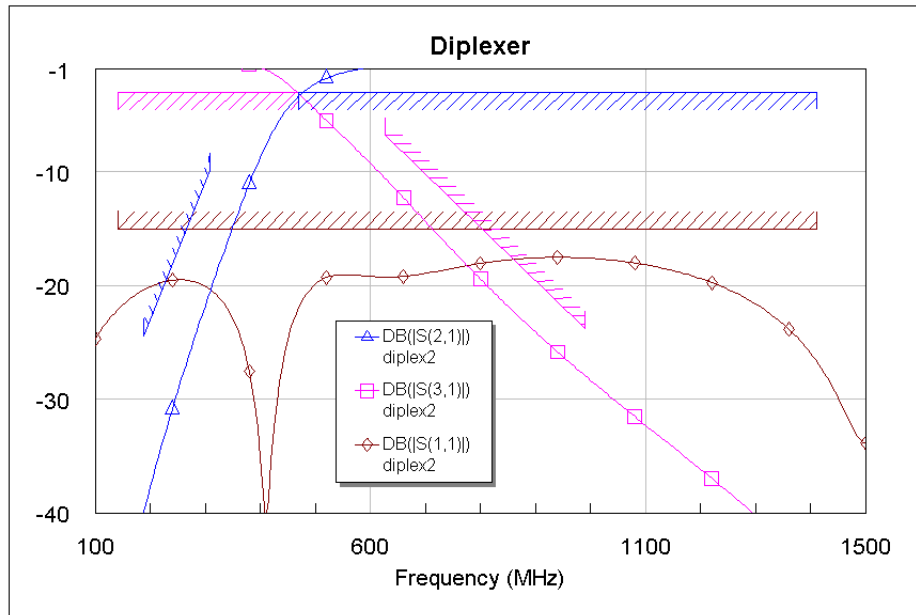


Figure 9: Frequency Response final circuit

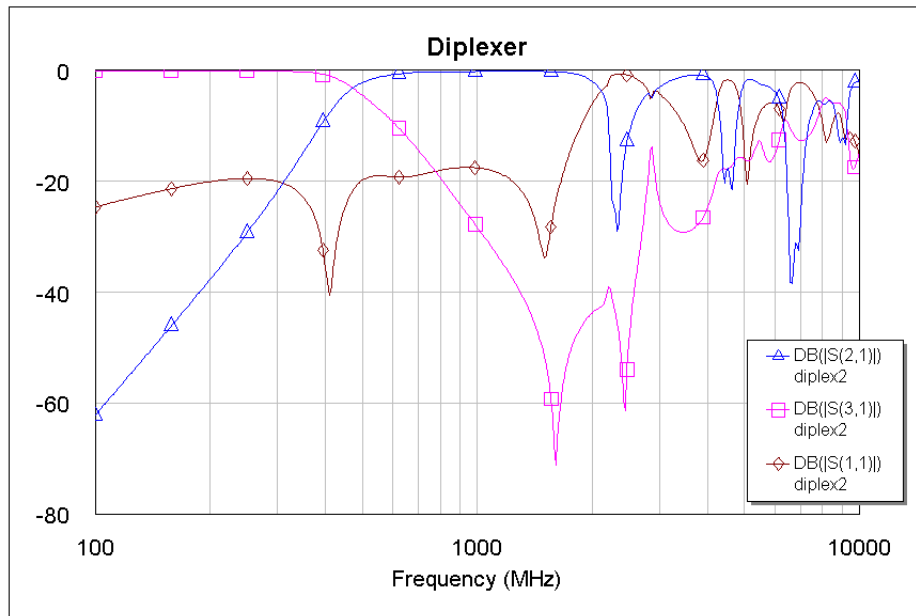


Figure 10: Frequency Response final circuit